## REMARKS

Applicants wish to thank Supervisory Examiner Le and Examiner Dole for the professional and courteous personal interview of January 27, 2003, with Applicants' representative. It is felt that this interview provided a better understanding of the position of the USPTO and, thereby, greatly expedited prosecution of this Application.

Entry of this Amendment is proper under 37 CFR §1.116 since no new claims are presented and no new issues are raised. Moreover, as demonstrated below, the rejection of record must be further clarified prior to proceeding to appeal. That is, the Examiner is respectfully requested to update the rejection of record to provide rationale consistent with the evaluation guidelines of MPEP §2100, thereby placing the rejection of record into condition for imminent appeal.

Applicants point out that the rejection of record inappropriately uses abstraction evaluation of patentability, rather than the MPEP guidelines. The current rejection of record, therefore, fails to meet the burden of a *prima facie* rejection under 35 USC §103(a).

Attached hereto is a marked up version of the changes made in the specification and claims by the current Amendment. The attached page is captioned **"Version with markings to show changes made."**

It is noted that the claim amendments herein are intended solely to more particularly point out the present invention for the Examiner, and not for distinguishing over the prior art or the statutory requirements directed to patentability. That is, Applicants wish to clarify that the present invention addresses an entirely different testing environment than that of a carrier containing electronic circuits or of a burn-in tester for integrated circuits.

Both of these latter testing environments involve carriers having electronic components already mounted thereon. The remaining independent claims are not further modified, since it is considered that they already adequately explicitly express this unique testing environment. Additionally, claim 7 is amended to expressly state that the open circuit condition is a fault condition. No such similar correction is needed for claim 10, since it clearly defines open circuits as being abnormalities.

It is further noted that, notwithstanding any claim amendments made herein, Applicant's intent is to encompass equivalents of all claim elements, even if amended herein or later during prosecution.

Claims 1-19 are all of the claims pending in the present Application. Claims 1-6 and 14-18 stand rejected under 35 USC §103(a) as unpatentable over US Patent 6,201,383 to Lo et al, further in view of US Patent 5,103,557 to Leedy. Claim 7 stands rejected under 35 USC §103(a) as unpatentable over Lo et al, further in view of US Patent 5,420,500 to Kerschner. Claim 8 stands rejected under 35 USC §103(a) as unpatentable over Lo et al, further in view of US Patent 5,438,272 to Craig et al. Claims 9-13 and 19 stand rejected under 35 USC §103(a) as unpatentable over Lo et al, further in view of Leedy, and further in view of Kerschner. These rejections are respectfully traversed in view of the following discussion.

## I. THE CLAIMED INVENTION

As described and claimed, e.g., by claim 1, the present invention is directed to an electronic circuit wiring interconnect package test and repair apparatus including at least one wiring analyzer to locate shorts between conductors on a surface of or embedded in a carrier substrate. The carrier substrate includes only conductors at the time of testing. These conductors are intended to interconnect components *that are not yet mounted* on the carrier substrate. A current source provides current sufficient to remove the shorts. At least two probes contact the conductors in a manner controlled by the wiring analyzer.

No cited prior art reference defines a test/repair apparatus for a wiring interconnect package, i.e., a carrier substrate having conductors to interconnect electronic components, wherein the carrier substrate is totally devoid of any such components at the time of testing as defined by the apparatus and process of the present invention.

Advantages of the present invention is that cost and time is considerably reduced for the manufacture of wiring interconnect packages.

## II. THE PRIOR ART REJECTION

The Examiner continues to maintain that US Patent 6,201,383 to Lo et al., further in view of US Patent 6,288,561 to Leedy, renders obvious the present invention as described by claims 1-6 and 14-18.

Applicants again respectfully submit that the rejection of record is improper, since it continues to ignore that the testing environment of the present invention differs entirely from that of the Lo and Leedy references. Claim 1 has been further amended to clarify this difference for the benefit of the Examiner by explicitly describing the testing apparatus as addressing wiring interconnect packages. As discussed during the interview of January 27, 2003, the state of the art for this testing environment differs from that of test sets used for testing fully completed electronic circuits and for testing integrated circuits.

Specifically, the state of the art for wiring interconnect package testing, as described on pages 1 and 2 of the specification, is that the repair of these packages requires a separate repair process and apparatus from that used to test for shorts or other defects. The present invention overcomes this problem, thereby providing the advantage of saving time and cost for the manufacture of these wiring interconnect packages.

The Lo reference, US Patent 6,201,383, clearly applies to a later stage of manufacturing. That is, it clearly applies to the specific testing to determine whether "short circuits exist among networks within a circuit under test" (see first line of Abstract, column 1 at lines 9-12, column 2 at lines 51-54, and all the independent claims 1, 2, 4, 6, 7, 10,19, and 21.

Applicants respectfully submit that, to one of ordinary skill in the art, the terminology "networks within a circuit" explicitly describes, by definition, a product that includes networks having electronic components already mounted. In contrast, the present invention addresses a problem of an earlier stage of manufacturing, i.e., before any components have yet been mounted on the substrate carrier.

Moreover, even if Lo is considered as an "analogous art", or if Lo were to be interpreted that the "networks" are equivalent to wires, under the guidelines of the MPEP,

beginning at MPEP §2141, the Examiner cannot simply ignore the teachings of this primary reference. That is, as the primary reference, Lo clearly teaches, at lines 5-8 of column 5, that any shorts identified be removed in a process separate from than that used to locate the short.

In MPEP §2141.02, it is clearly stated: "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention" (emphasis in MPEP). In MPEP §2143.01, the evaluation guideline is clearly stated: "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination" (emphasis in MPEP). Again, it is clear that Lo, at lines 5-8 of column 5, clearly teaches against the combination urged by the Examiner.

Therefore, Applicants respectfully submit that the rejection on record is improper by ignoring the explicit teaching in the primary reference that teaches against the urged combination.

To overcome this basic deficiency of Lo, the Examiner introduces Leedy. The Examiner asserts that "it would have been obvious to one skilled in the art at the time of the invention to use the current source of Leedy in the apparatus of Lo et al. for the additional purpose of removing shorts and repairing electronic circuits since it is stated by Lo et al. that "it is desirable to determine which networks are shorted together, so that the circuit can be repaired" (column 6, lines 54-56)."

Applicants first point out that this statement in Lo falls short of suggesting that the short-isolation detection apparatus further include the capability of repairing the identified shorts between circuit networks. Indeed, at lines 5-8 of Lo, the opposite suggestion is made: "The results of the testing process are displayed on a display screen 50, and may be used in other ways, such as the diversion of failing components into a scrap bin." Absent hindsight, there is no way that this phraseology can reasonably be interpreted as suggesting that the Lo apparatus be modified to include an automatic short-circuit repair process.

Indeed, assuming that Lo is interpreted as being analogous art, then it more reasonably is interpreted as confirming that the art continues to suffer the problem that shorts are NOT removed by the apparatus that is used to detect their presence. That is, if Lo is an analogous or equivalent art, it clearly confirms the Applicants' description on pages 2 and 3

of the specification that the art lacks a method to repair detected shorts using the short-detecting apparatus. The Examiner cannot simply ignore this clear confirmation and simply decide that it would be obvious to overcome a problem that is not even further discussed in the primary reference.

By combining Leedy with Lo, the Examiner is even more clearly crossing boundaries between arts. That is, Leedy clearly applies to integrated circuits (see Title, first sentence of the Abstract, and line 37 of column 3). Indeed, as clearly described at lines 51-54 of column 3, Leedy applies only to finished IC wafers. Such wafers are entirely different from wiring interconnect packages. It is noted that line 6 of column 5 of Leedy refers to a cluster probe having over 500,000 probes for full-wafer tests, indicating very clearly a testing environment entirely different from wiring interconnect packages.

Stating slightly differently how the art of the present invention clearly differs from that of Leedy, it is well known that once the IC wafer has been sliced into IC dies and a die has been properly installed in an appropriate package, the resultant IC module may well become one of the electronic components that are missing on the wiring interconnect package addressed by the present invention.

In general, the present rejection incorrectly evaluates patentability by extracting a missing feature from an entirely different environment and then applying this isolated feature as an abstraction. That is, in direct contradiction of the MPEP guideline that the prior art itself must suggest a modification, according to the abstraction approach of the current rejection, once a feature is described in some art, it then becomes obvious to import this feature anywhere else.

The motivation to combine references under this evaluation technique will always be: "It would be obvious to modify the primary reference to incorporate the abstracted feature of a secondary reference, since the primary reference would receive the benefit described by the abstraction".

The basic flaw with this technique is that it blatantly ignores the above-mentioned guideline in MPEP §2143.01: "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination" (emphasis in MPEP).

Stated slightly differently, this technique of simply combining features based on abstraction defeats entirely the intended purpose of the patent system, wherein it is a well-established doctrine that a new combination of known elements may very well provide a non-obvious advance.

Moreover, even if Leedy is combined with Lo, the combination would still fail to produce the combination described in various claims.

Specifically, the Examiner is understood as relying upon Leedy for demonstrating a "solid state analyzer". Having presumably decided that the isolated element of a "solid state analyzer" in Leedy automatically renders a solid state analyzer obvious in any environment (presumably because of speed), the Examiner then relies upon line 49 of column 5 and lines 52-54 of column 5 of Leedy as suggesting that two analyzers (presumably a relay analyzer and a solid state analyzer) is rendered obvious by the solid state analyzer in Leedy.

However, a reasonable interpretation of the full description behind these lines in column 5 has nothing whatsoever to do with a second wiring analyzer, i.e., a solid state analyzer optionally installed as a faster version of a relay analyzer to detect the shorts and the relay analyzer invoked to perform the repair because higher currents and/or voltages are required for the repair.

That is, a fair reading of column 5 of Leedy provides no indication or suggestion whatsoever of a second wiring analyzer, let alone a first, slower relay wiring analyzer required to apply high voltages and currents for repairs, plus an optional, second, high speed solid state wiring analyzer that would provide speed alone without having value to execute repairs.

A fair reading of the paragraph at lines 37-54 of column 5 has no suggestion of anything except a single analyzer for each wafer type being tested (see lines 37-38: "... and IC circuitry 50 that are specific for a wafer being tested"). Indeed, the next line refers to the option of being able to automatically exchange this analyzing circuitry when the type of wafer is changed (lines 38-40), and the next sentence even expressly confines the IC circuitry 50 as being either solid state or exclusively incorporating only passive elements (line 43). The two following sentences (lines 44-51) confirm this interpretation of having one or the other of two possible embodiments. Clearly, there is no suggestion whatsoever of having,

first, a relay wiring analyzer and, optionally, including a second, solid state wiring analyzer for speed.

As best understood by Applicants' representative during the interview of January 27, the Examiner relies on the phraselogy "The *incorporation of active device switching circuitry* into probing devices would create intelligent and programmable probing devices" (lines 52-54 of column 5) as somehow justifying that Leedy suggests having two separate wiring analyzers. However, Applicants respectfully submit that the plain English of these words fall short of even hinting at such configuration.

In the fourth full paragraph of page 4 of the Office Action, the Examiner says: "Therefore, it would have been obvious ... to incorporate the controller of Leedy into the apparatus of Lo et al. for the purpose of automatically positioning the probes to reduce the possibility of human error or further damage due to additional handling." The problem with this rationale is that it ignores that Lo already has a controller (see Figure 1, item 40) that performs exactly this function. Therefore, there is no need to modify Lo to change its controller 40.

In the final paragraph of page 4, the Examiner alleges that Leedy discloses a controller for a voltage stress test, pointing to the description at lines 60-63 of column 6.

However, a fair reading of these lines indicates nothing more than the factual statement that higher voltages may be necessary for the higher currents that would be required for burning out shorts. It is well known that voltage is required to drive current, so that this statement provides no hint whatsoever of a suggestion to perform a high voltage stress test. "Stress test" has a specific meaning in the present invention and arises because the present invention address an art entirely different from that of either Lo or Leedy, i.e., the art of testing wiring interconnect packages.

Relative to the rejection for claim 7, the Examiner concedes that Lo fails to provide the capability to locate open circuits, and introduces Kerschner.

The problem with this rejection is that the Examiner again ignores the MPEP guidelines by forgetting that the purpose of the primary reference Lo would be entirely defeated if this feature would be added. The Lo apparatus exists for the sole purpose of "determining whether short circuits exist among networks within a circuit under test" (see

first sentence of Abstract). It achieves this determination by measuring the amount of current that flows when voltage is applied between two test points (column 4 at lines 47-57). There is no suggestion in Lo to search for open circuits.

In Lo, if the networks have no short circuits between networks, an open circuit inherently exists. The open circuit is the expected result if the testing is successful. There is no suggestion whatsoever in Lo to reverse this expected result of an open circuit being the abnormality being sought. The Examiner cannot simply ignore this teaching in the primary reference Lo.

According to MPEP 2143.01, the Examiner cannot combine references if the combination either renders the prior art unsatisfactory for its intended purpose ("If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification.") or changes the principle of operation of a reference ("If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teaching of the references are not sufficient to render the claims *prima facie* obvious.")

The rejection currently of record ignores both these guidelines. First, it ignores that the primary reference uses the detection of an open circuit as determining that the network interface is normal, i.e., no shorts. Second, the underlying principle of the primary reference Lo consists of measuring the amount of current passing between two test points. In contrast, the secondary reference Kerschner uses a capacitance technique that is totally inconsistent with the simple current measurement circuit described at lines 47-57 of column 4 of Lo. To measure open circuits as taught by Kerschner, the Lo apparatus would have to be drastically modified. Therefore, for either of these two reasons, Kerschner cannot be combined with Lo.

Relative to the rejection currently of record for claim 8, again the guidelines in MPEP 2143 are ignored. That is, the Examiner concedes that Lo fails to teach or suggest the claimed feature that multiple attempts are made to remove shorts and introduces Craig, pointing to lines 39-55 of column 8.

However, a fair reading of these lines indicates no relation whatsoever to the claimed subject matter. That is, the process described in these lines concerns the determination of

whether a short circuit exists. It has nothing whatsoever to do with attempting to remove an identified short circuit.

As Applicants have repeatedly stated on the record, the present invention addresses a problem in the technical area of testing/repairing wiring interconnect packages, i.e., a substrate carrier having conductors but totally devoid of electronic components. The present invention addresses the problem in that art by combining the repair of these wiring interconnect packages into the same apparatus used to detect the faults. As described by Applicants on pages 1 and 2 of the specification and, if Lo is considered as analogous or equivalent art, by the primary reference itself, this problem has not been solved.

The rejection on record clearly ignores the guidelines of the MPEP by taking elements totally outside the art and totally out of context, thereby attempting to "kludge together" the present invention as described by the claims.

Advantages of providing an automated short circuit removal technique into the apparatus used to test for and isolate the short circuits include considerable savings in time and cost and considerable savings in scrapped materials.

Hence, turning to the clear language of the claims, there is no teaching or suggestion of "[a]n electronic circuit *wiring interconnect package* test and repair apparatus ... at least one wiring analyzer to locate shorts between conductors, ... said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit, said carrier substrate being devoid of all said components; a current source to provide current sufficient to remove said shorts ...," as clearly required by claim 1. Independent claims 9, 11, 14, and 19 have corresponding terminology "interconnect packages".

For this reason alone, the claimed invention is fully patentable over the cited references.

For any of the reasons stated above, the claimed invention is fully patentable over the cited references.

Further, the other prior art of record has been reviewed, but it too even in combination with the Lo, Leedy, Kerschner, or Craig, fails to teach or suggest the claimed invention.

## IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-19, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview. The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0458.

Respectfully Submitted,

Date: 2/25/03

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**VERSION WITH MARKINGS TO SHOW CHANGES MADE**

IN THE CLAIMS:
**The claims have been amended, as follows:**

1. (Amended) An electronic circuit wiring interconnect package test and repair apparatus, comprising:

at least one wiring analyzer to locate shorts between conductors, said conductors being on a surface of or embedded in a carrier substrate, said conductors being intended to interconnect components to be mounted on said carrier substrate to form a circuit, said carrier substrate being devoid of all said components;

a current source to provide current sufficient to remove said shorts; and

at least two probes to contact said conductors in a manner controlled by said wiring analyzer.

7. (Amended) The test and repair apparatus of claim 1, wherein said at least one wiring analyzer additionally locates open circuits that are defects in said carrier substrate.